R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

Applicant thanks Examiner Pham for the indication of allowable matter in the claims 3-10 and 13-19.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 4 lines 3-6, page 4 line 15-page 5 line 4, page 6 lines 17-20 and FIG. 1, as originally filed. The new claims are split from claims 6, 7, 16 and 17. Thus, no new matter has been added.

OBJECTION TO THE DRAWINGS

The objection to the drawings because of illegible print is respectfully traversed and should be withdrawn. The copy of the figures available to Applicant's representative appear to be legible. Unfortunately, the Examiner's copy of the figures are not available to Applicant's representative. Therefore, Applicant's representative has no means to determine what text is considered not clearly legible. As such, the Examiner is respectfully requested to either (i) specifically identify which text in which figures is unclear or (ii) withdraw the objection. Applicant's plan to file a formal set of drawings after the application has been allowed.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 2, 11, 12 and 20 under 35 U.S.C. §103(a) as being unpatentable over Duesman '111 in view of Albachten et al. '247 (hereafter Albachten) has been obviated in part, is respectfully traversed in part, and should be withdrawn.

Duesman concerns a charge pump disablement apparatus (Title). Albachten concerns a system for accessing the same memory location by two different devices (Title).

Claim 1 provides a bit cell configured to generate a bit signal having a fixed logic value. In contrast, both Duesman and Albachten appear to be silent regarding fixed value bit signals. Therefore, Duesman and Albachten, alone or in combination, do not appear to teach or suggest a bit cell configured to generate a bit signal having a fixed logic value as presently claimed.

Claim 1 further provides a sense amplifier configured to generate a reset signal in response to sensing said bit signal. Despite the assertion on page 3 of the Office Action, Duesman appears to contemplate that a sense amplifier enable signal is received by a sense amplifier. In particular, Duesman states in column 3, lines 3-6:

> ...**said memory** generating a row selection signal to select a row of memory cells and **generating a sense amplifier enable signal to activate said sense amplifier**... (Emphasis added)

Duesman states that **the memory**, not the sense amplifier, generates the sense amplifier enable signal. Therefore, Duesman and Albachten, alone or in combination, do not appear to teach or

suggest a sense amplifier configured to generate a reset signal in response to sensing said bit signal as presently claimed.

Claim 1 further provides a control circuit configured to (i) set a control latch in response to a detection signal and (ii) reset the control latch in response to a reset signal, wherein the control latch is set while both the detection signal and the reset signal are in an asserted state to halt a self-timed read cycle. In contrast, both Duesman and Albachten appear to be silent regarding setting a control latch to halt a self-rimed read cycle. Therefore, Duesman and Albachten, alone or in combination, do not appear to teach or suggest a control circuit configured to (i) set a control latch in response to a detection signal and (ii) reset the control latch in response to a reset signal, wherein the control latch is set while both the detection signal and the reset signal are in an asserted state to halt a self-timed read cycle as presently claimed. Claims 11 and 20 provide language similar to claim 1. As such, claims 1, 11 and 20 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 2 provides a detection circuit configured to generate the detection signal in the asserted state in response to detecting a transition of an address signal. In contrast, Duesman appears to be silent regarding assertion of a Row Selection signal (asserted similar to the claimed detection signal) in response to **detecting a transition** of an address signal. Therefore, Duesman and Albachten, alone or in combination, do not appear to teach or suggest a detection circuit configured to generate a detection

signal in an asserted state in response to detecting a transition of an address signal as presently claimed. Claim 12 provides language similar to claim 2. As such, claims 2 and 12 are fully patentable over the cited references and the rejection should be withdrawn.

Applicant's representative respectfully traverses the assertion on the top of page 4 of the Office Action that a row selection signal is inherent from row address decoding. MPEP §2112 states:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. " *Ex parte Levy* 17 USPQ2d 1461, 1464, 1464 (Bd. Pat. App. & Inter. 1990)(emphasis in original)

However, no evidence or convincing line of reasoning has been provided in the Office Action. Therefore, inherency has not been established and the assertion should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829

Dated: May 16, 2005

c/o Peter Scott
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

Docket No.: 02-241 / 1496.00187